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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,468	KATAYAMA, YOSHIAKI	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by RONKKA (U.S. Patent 6,631,394).

As to claim 1, RONNKA teaches a processor power-saving control method which employs a plurality of Operating Systems (first operating system / second operating system) whose execution is controlled by a processor (processor) (col. 9, lines 37-60), wherein the plurality of OS include: a primary OS (first operating system) for receiving a timer interrupt (timer interrupt) issued from a hardware timer after a predetermined time lapse (via sending the processor an interrupt message to handle) (col. 14, lines 14-29; col. 16, lines 20-31; col. 16, lines 41-49; col. 24, lines 15-20), and a secondary OS (second operating system) treated as a task (thread) to be executed by the primary OS (col. 29, lines 43-45), the processor power-saving control method comprising the steps of: upon receiving the timer interrupt at the primary OS, determining with the primary OS whether there exists any task to be executed on the secondary OS executed (determining whether there are no threads of the first operating system waiting for

execution / determining the thread that is to handle the interrupt) (col. 24, lines 5-29; col. 21, lines 3-39; col. 15, line 30 – col. 16, line 20); and when the primary OS determines there exists any task to be executed on the secondary OS, interrupting the secondary OS by issuing a secondary OS interrupt from the primary OS to the secondary OS (via passing the interrupt data to the second operating system so that the thread is executed) (col. 28, lines 65-67; col. 17, lines 1-19; col. 14, lines 58-63) (via after executing the interrupt service routine, executing the other threads until there is no thread ready to run or another interrupt occurred) (col. 16, lines 6-31).

As to claim 14, RONKKA teaches activating the secondary OS (second operating system) from a sleep mode (via the operating system stopping the execution of its idle thread to execute the interrupt service routine and any other higher priority threads) in response to the secondary OS receiving the secondary OS interrupt issued from the primary OS (col. 16, lines 6-31).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over RONKKA (U.S. Patent 6,631,394).

As to claim 2, RONKKA teaches a processor power-saving control method which employs a plurality of Operating Systems (first operating system / second operating system) whose execution is controlled by a processor (processor) (col. 9, lines 37-60), the processor power-saving control method controlling timer interrupt processing performed by a hardware timer (timer) which activates the processor after an arbitrary time lapse (via sending the processor an interrupt message to handle), the processor power-saving control method keeping a power-saving state of the processor (via providing a longer operation time by using a single battery charge) (col. 3, lines 26-28), the plurality of OS including a primary OS (first operating system) for receiving a timer interrupt (interrupt) issued from the hardware timer (col. 14, lines 14-29; col. 16, lines 20-31; col. 16, lines 41-49; col. 24, lines 15-20) and a secondary OS (second operating system) treated as a task (thread) to be executed by the primary OS (col. 29, lines 43-45), the processor power saving control method comprising: a primary OS process step performed by the primary OS; a secondary OS process step performed by the secondary OS; and a secondary OS interrupt step, the primary OS process step including: detecting the timer interrupt (receiving the interrupt), a first determination step of, upon receiving the timer interrupt, determining whether there exists any task to be executed (determining whether there are no threads of the first operating system waiting for execution) (col. 24, lines 5-29; col. 21, lines 3-39; col. 15, line 30 – col. 16, line 20); the secondary OS process step including a second determination step of determining whether there exists any task to be executed (determining whether there are no threads of the second operating system waiting for execution) (col. 16, lines 6-

31), and when there is no task to be executed, handing over processing to the first determination step (via switching back to the first operating system at any phase) (col. 16, lines 6-31); the secondary OS interrupt step including receiving a secondary OS interrupt from the primary OS (via passing the interrupt data to the second operating system) (col. 28, lines 65-67; col. 17, lines 1-19; col. 14, lines 58-63), when the first determination step has determined that there exists any task to be executed on the secondary OS (determining that a particular thread should be executed based on the interrupt), performing interrupt processing on the secondary OS (via executing the interrupt service routine by the second operating system), and executing the second determination step at a predetermined time measured from the interrupt (via after executing the interrupt service routine, executing the other threads until there is no thread ready to run or another interrupt occurred) (col. 16, lines 6-31).

However, RONKKA does not explicitly mention that the operation of the processor being stopped when there exists no task to be executed on the OS's. Official Notice is taken in that it is well known to one of ordinary skill in the art that a processor is active, and thereby running when tasks are assigned or ready to the processor for execution and when there is no task assigned or ready to the processor for execution, the processor is in an inactive, stopped or stand by state and thereby not executing. Hence the processor is stopped. In addition, when the processor is stopped it would not be using any power of the system and thereby saving the power of the system. Therefore, it would be obvious to one of ordinary skill in the art at the time of the

invention that the processor of RONKKI would stop **if** a task were not available to execute.

As to claim 10, reference is made to a computer readable storage medium that correspond to the method of claim 2 and is therefore met by the rejection of claim 2 above.

As to claim 11, reference is made to a device that corresponds to the method of claim 2 and is therefore met by the rejection of claim 2 above.

As to claim 15, 16, and 17, RONKKA teaches activating the secondary OS (second operating system) from a sleep mode (via the operating system stopping the execution of its idle thread to execute the interrupt service routine and any other higher priority threads) in response to the secondary OS receiving the secondary OS interrupt issued from the primary OS (col. 16, lines 6-31).

As to claim 3, RONKKA teaches the secondary OS interrupt step is executed by a periodically-activating handler (interrupt handler) which interrupts the secondary OS (via the interrupts received by a timer) (col. 16, line 61 – col. 17, line 19) (col. 14, lines 14-29; col. 16, lines 20-31; col. 16, lines 41-49; col. 24, lines 15-20). Official Notice is taken in that periodic timers are well known in the art and therefore would be obvious to

one of ordinary skill in the art that the timer is a periodic timer for interrupting and thereby executing the secondary OS.

As to claim 4, RONKKA teaches the secondary OS interrupt step is executed by an alarm handler (interrupt handler) which interrupts the secondary OS (via the interrupt received by a timer) (col. 16, line 61 – col. 17, line 19) (col. 14, lines 14-29; col. 16, lines 20-31; col. 16, lines 41-49; col. 24, lines 15-20). Official Notice is taken in that time of day timers are well known in the art and therefore would be obvious to one of ordinary skill in the art that the timer is a time of day timer that generates an interrupt at a specific time.

As to claim 5, RONKKA teaches the secondary OS interrupt step is executed by a high priority task (super thread / interrupt service routine) which is a task for interrupting the secondary OS and has a highest priority order among tasks to be executed by the primary OS (via executing the interrupt service routine first and then the other threads) (col. 15, line 54 – col. 16, line 31; col. 21, line 3-39; col. 24, lines 5-29).

As to claim 6, RONKKA teaches a step of determining whether time taken until the hardware timer issues a next timer interrupt (response time) is longer than a predetermined time (execution time), and if a measured time is longer than the predetermined time, the processor stopping step stops operation of the processor (via increasing the priority of the idle thread such that the idle thread is executed and

thereby there is no task to execute on the processor such that a processor without a task would stop executing) (col. 24, lines 5-29).

As to claims 7-9, RONNKA substantially teaches the invention of receiving a plurality of different timer interrupts and processing accordingly. However, RONNKA does not teach that the timer is a long-periodic timer or a time of day timer. Official Notice is taken in that it is well known in the art to one of ordinary skill in the art that a timer can be a time of day timer that generates an interrupt at a specific time and a timer that generates an interrupt after a longer period than another timer, hence a long-periodic timer and therefore such timers would obviously be used in the teachings of RONNKA in order to handle interrupts in a multi-operating system fashion. In addition, it would be obvious to one of ordinary skill in the art that a programmer can program a timer to generate an interrupt at a particular time in any fashion and can remove such an interrupt generation indication so that the timer does not generate an interrupt also.

As to claims 12 and 13, RONNKA substantially teaches the invention of receiving a plurality of different timer interrupts and processing accordingly. However, RONNKA does not teach that the timer is a long-periodic timer or a time of day timer. Official Notice is taken in that it is well known in the art to one of ordinary skill in the art that a timer can be a time of day timer that generates an interrupt at a specific time and a timer that generates an interrupt after a longer period than another timer, hence a long-

periodic timer and therefore such timers would obviously be used in the teachings of RONNKA in order to handle interrupts in a multi-operating system fashion.

Response to Arguments

3. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 20, 2006

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER